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Commissioner for Patents
Amendment dated January 24, 2005
Response to Office Action dated September 22, 2004
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Serial No.: 10/054017
Art Unit: 2113
Examiner: Baderman
Docket No.: RPS9 2001 0090 US1

REMARKS/ARGUMENTS

Claims 1-20 were presented and examined. The Examiner objected to informalities in claims 1 and 20. The Examiner rejected claims 1-2, 4-6, 10-11, 13-15, 17 and 18 under 35 USC § 102(b), as being anticipated by Bouvier *et al.* (U.S. Patent No. 5,530,946), hereinafter "Bouvier". Claims 1-20 were rejected under 35 USC § 102(e), as being anticipated by Bossen *et al.* (U.S. Patent No. 6,233,680). The Examiner rejected claims 7-9, 16 and 20 under 35 USC § 103(a), as being unpatentable over Bouvier.

Claim Objections

The Examiner objected to informalities in claims 1 and 20. In response, Applicant has amended claim 1 to address the informality and canceled claim 20. Applicant submits that the claim 1 as amended addresses the objection raised by the Examiner and Applicant would respectfully request the Examiner to reconsider and withdraw the objection.

Claim rejections under 35 USC §§ 102(b), 102(e)

The Examiner rejected claims 1-2, 4-6, 10-11, 13-15, 17 and 18 under Section 102(b) as being anticipated by Bouvier and claims 1-20 under Section 102(e) as being anticipated by Bossen. In response, Applicant has canceled claims 17-20 and amended independent claims 1 and 10 to recite that the error detection logic is external to the main processors and that the claimed system includes a service processor and that the error logic includes a status register that is accessible via an I2C bus. Support for the external logic limitation is found in FIG 1 and the corresponding text beginning on page 6, line 6 and following. Support for the service processor limitation is found in FIG 1 and supporting text beginning on page 7 line 20 and following. Support for the error status register and I2C limitations is found in FIG 2 and the supporting text at page 8, line 1 and following.

The references do not anticipate or suggest the limitations of claim 1 as amended. Anticipation requires that all claimed limitations are found either explicitly or inherently in a single reference. The cited references do not anticipate claim 1 as amended because neither of the cited references teaches dedicated error logic that is external to the system processors and

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includes an I2C accessible error status register. Neither Bouvier nor Bossen discloses an I2C accessible status register as part of its error detection logic. Nor is there any suggestion or motivation found in the references themselves to modify the references to include an I2C limitation. The use of an I2C accessible error status register beneficially enables external access to the error detection logic in the event that the information is not otherwise accessible via the conventional I/O busses. Because this limitation is neither taught nor suggested by the cited references, Applicant would respectfully request the Examiner to reconsider and withdraw the anticipation and obviousness rejections of independent claim 1 as amended. Analogous arguments apply to claim 10 as amended.

In this response, Applicant has addressed the Examiner's objections and claim rejections under 35 USC § 102(b), second paragraph, 35 USC § 102(e), and 35 USC § 103(a). Accordingly, Applicant believes that this response constitutes a complete response to each of the issues raised in the office action. In light of the amendments made herein and the accompanying remarks, Applicant believes that the pending claims are in condition for allowance. Accordingly, Applicant would request the Examiner to withdraw the rejections, allow the pending claims, and advance the application to issue. If the Examiner has any questions, comments, or suggestions, the undersigned attorney would welcome and encourage a telephone conference at 512.428.9872.

Respectfully submitted,



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